Final Technical Program

Third International Silicon-Germanium Device and Technology Meeting (ISTDM)
May 15 -17, 2006
Princeton University
Princeton, NJ 08540 USA

Sunday, May 14, 2006

Reception and Registration
7:00 PM – 9:00 PM, Prospect House

Monday, May 15, 2006

Registration and Breakfast
8:00 AM – 9:00 AM, Friend Center 113

9:00 – 9:15 Introduction – Friend 101

Session I: Plenary Session – Friend 101

9:15 – 9:55 1.1 Discontinuous Innovation: Strained Silicon Technology, Gary L. Patton; IBM Systems and Technology Group, 2070 Route 52, Hopewell Junction, NY, 12533 USA

9:55 – 10:35 1.2 Silicon Microphotonics: Hardware for the Information Age, Lionel C Kimerling; Massachusetts Institute of Technology, 77 Massachusetts Ave, Cambridge, MA, 02139, USA

Break
10:35 AM – 10:55 AM, Friend 113

[Parallel Session]
Session II: Strained Si FET/CMOS and Technology
10:55 AM – 11:55 AM, Friend 101

10:55: 2A.1 **Performance Boosting of Peripheral Transistor for High Density 4Gb DRAM Technologies by SiGe Selective Epitaxial Growth Technique**, I. S. Jung[1]; S.-G. Lee[1]; D.-H. Lee[1]; E.-C. Lee[2]; W. Kim[3]; P.K. Kang[1], Y.-H. Son[1]; S.-K. Kang[1]; J.-B. Kim[1]; Y.-P. Kim[1]; K.-H. Lee[1]; M.-G. Kang[1]; H. Kim[1]; J.-W.Lee[1]; Y.G. Shin[1]; U-I. Chung[1] and J.T. Moon[1]; [1] Process Development Team, Memory Division, Semiconductor Business, Samsung Electronics Co., Ltd. 449-711 San#24 Nongseo-Dong, Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea; [2] Technology Development Team, Memory Division, Semiconductor Business, Samsung Electronics Co., Ltd. Korea; [3] Device Research Team, Memory Division, Samsung Electronics Co., Ltd. Korea

11:10: 2A.2 **Thick-Strained-Si/SiGe CMOS Technology with Selective-Epitaxial-Si Shallow-Trench Isolation (SES-STI)**, M. Miyamoto[1]; N. Sugii[2]; Y. Yoshida[1], Y. Hoshino[3]; Y. Kimura[2], M. Kondo[3] and K. Ohnishi[3], [1] Micro Device Division, Hitachi, Ltd., 16-3, Shinmachi 6-chrome, Ome-shi, Tokyo 198-8512 Japan; [2] Central Research Laboratory, Hitachi, Ltd.; [3] Renesas Technology Corp. Japan

11:25: 2A.3 **p-n Junction Leakage Current in Strained-Si/SGOI Diodes**, A. Tanabe[1]; T.Numata[1]; T. Tezuka[1]; N. Hirashita[1]; S.Takagi[2]; [1] MIRAI, Association of Super-Advanced Electronics Technology (ASET), 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 212-8582, Japan; [2] MIRAI, Advanced Semiconductor Research Center (ASRC), National Institute of Advanced Industrial Science and Technology (AIST) Japan

11:40: 2A.4 **Impact of Etching Depth on the Leakage Current of Recessed SiGe Junctions**, M. Bargallo Gonzalez[1]; G. Eneman[1,2,3]; P. Verheyen[1]; C. Claeys[1,2]; A. Benedetti[1]; H. Bender[1]; K. De Meyer[1,2]; E. Simoen[1]; R. Schreutelkamp[4]; L.Washington[4]; F. Nouri[4]; [1]IMEC, Kapeldreef 75, B-3001, Leuven, Belgium; [2] ESAT-INSYS, K.U. Leuven, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium [3]Research Assistant of The Fund for Scientific Research – Flanders, Belgium, [4]Applied Materials, Sunnyvale, CA, USA

[Parallel Session]
Session 2B: Germanium Device Technology
10:55 AM – 11:55 AM, CS 104

10:55: 2B.1 **Germanide phase formation and texture**, Simon Gaudet[1]; Christian Lavoie[1,3]; Christophe Detavernier[2]; Patrick Desjardins[1]; [1]Departement de Génie physique, Ecole Polytechnique de Montreal, P.O. Box 6079, Station Centre-Ville, Montreal, Quebec, H3C 3A7, Canada; [2]Department of Solid State Physics, Ghent University, Ghent, Belgium; [3]IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, USA

11:10: 2B.2 **Accurate Modelling of Average Phosphorus Diffusivities in Germanium after Long Thermal Anneals**, Malcolm Carroll; R. Koudelka; Sandia National Labs, P. O. Box 5800, M. S. 1077, Albuquerque, NM, 87185, USA

11:25: 2B.3 **Strained Pt Schottky Diodes on n-type Si and Ge**, M. H. Liao[1]; S. T Chang[2]; P. S Kuo[1]; H.-T Wu[1]; C.-Y Peng[1]; C. W Liu[1]; [1]Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan R.O.C.; [2]Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan R.O.C.

11:40: 2B.4 **Negative Differential Resistance in Ultra-Thin Ge-On-Insulator FETs**, D. Kazazis[1]; A. Zaslavsky[1]; E. Tutuc[2]; N.A. Bojarczuk[2]; S. Guha[2]; [1]Division of Engineering, Brown University, 182 Hope St., Providence, RI, 02912, USA; [2] IBM T. J. Watson Research Center, P.O Box 218, Yorktown Heights, NY, 10598, USA

Lunch
12:00 PM – 1:30 PM, Friend 113

Session 3: Invited: Optoelectronics and Ge FET's
1:30 PM – 3:30 PM, Friend 101

1:30: 3.1 **Ge/SiGe Quantum Confined Stark Effect Modulators on Silicon**, James S Harris; Yu-Hsuan Kuo; David A.B. Miller; Stanford University, Solid State and Photonics Lab, CISX 328, Stanford, CA, 94305, USA

2:00: 3.2 **Performance and Reliability of SiGe Photodetectors**, Mike Morse[1]; Femi Dosunmu[2]; Yoel Ghetrit[3]; Gadi Sarid[3]; [1] Intel Corporation, 2200 Mission College Blvd, Santa Clara, CA, 95053, USA; [2] Intel Corporation, 2200 Mission College Blvd, Santa Clara, CA, 95053, USA; [3] Intel Corporation, S.B. I Park Har Hotzvin, Jerusalem, 91031, Israel

2:30: 3.3 **Ge deep sub-micron HiK/MG pFET with superior Drive compared to Si HiK/MG state-of-the-art reference**, B. De Jaeger[1]; B. Kaczer[1]; P. Zimmerman[2]; K. Opsomer[3]; G. Winderickx[3]; J. Van Steenbergen[3]; E. Van Moorhem[3]; R. Bonzom[3]; F. Leys[3]; C. Arena[4]; M. Bauer[4]; C. Werkhoven[4]; M. Meuris[5]; Marc Heyns[5]; [1] IMEC, Kapeldreef 75, B-3001 Leuven, Belgium; [2] Intel; [3] IMEC; [4] ASM America, 3440 E. University Drive, Phoenix, Ar, 85034; [5] IMEC, Belgium

3:00: 3.4 **III-V/Si Device Integration Via Metamorphic SiGe Substrates**, Steven A Ringel[1]; Ojin Kwon[2]; Matthew Lueck[1]; John Boeckl[3]; Eugene Fitzgerald[4]; [1] Dept. of Electrical and Computer Engineering, The Ohio State University, 2015 Neil Ave, Columbus, OH, 43210, USA; [2] Lumileds, Inc., San Jose, CA, 95136, USA; [3] Air Force Research Laboratory, Wright Patterson AFB, Dayton, OH 45433 USA; [4] Dept. of Materials and Science and Eng., Massachusetts Institute of Technology, Cambridge, MA 02139, USA

Break
3:30 PM – 3:50 PM, Friend 113

[Parallel Session]
Session 4A: Optoelectronics
3:50 PM – 4:50 PM, Friend 101

3:50: 4A.1 **Fast Ge p-i-n photodetectors on Si**, E. Kasper[1]; M. Oehme[1]; J. Werner[1]; M. Jutzi[2]; M. Berroth[2]; [1]Institut fur Halbleitertechnik, University of Stuttgart, Pfaffenwaldring 47, 70569, Stuttgart, Germany, [2]Institut fur Elektrische und Optische Nachrichtentechnik, University of Stuttgart, Germany

4:05: 4A.2 **Ge/Si (100) Heterojunction Photodiodes Grown by Low-Energy Plasma-Enhanced CVD**, Giovanni Isella[1,2] Johann Osmond[1]; Matthias Kummer[2]; Rolf Kaufmann[3]; Hans von Kaenel[1,2]; [1]L-NESS Politenico di Milano – Polo di Como Via Anzani 52, 22100 Como Italy; [2]Epispeed AG Technoparkstrasse 1, 8005 Zurich Switzerland, [3]Centre Suisse d'Electronique et de Microtechnique SA Badenerstrasse 569, 8048 Zurich, Switzerland

4:20: 4A.3 **MBE growth and characterization of three-terminal Ge(dot)/SiGe(well) near-infrared photodetectors**, A.Elfving; A. Karim; M. Zhao; G. V. Hansson; W.-X. Ni; Department of Physics, Chemistry and Biology, Linköping University, 581 83 Linköping, Sweden

4:35: 4A.4 **Fabrication of Silicon on Lattice-Engineered Substrate (SOLES) as a Platform for Monolithic Integration of CMOS and Optoelectronic Devices**, Carl L Dohrman; Kamesh Chilukuri; David M Isaacson; Minjoo L Lee; Eugene A Fitzgerald; Department of Materials Science and Engineering, Massachusetts Institute of Technology (MIT), 77 Massachusetts Ave, Rm

13-4154, Cambridge, MA, 02139, USA

[Parallel Session]
Session 4B: Ge MIS/MOS Technology
3:50 PM – 4:50 PM, CS 104

3:50: 4B.1 **Temperature-Dependent Admittance Analysis of HfO_2 Gate Dielectrics on Nitrogen- and Sulfur-passivated Ge**, Steven J Koester[1]; Martin M Frank[1]; David M Isaacson[1,2]; Huiling Shang[1]; [1] IBM, T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY, 10598, [2]Department of Materials Science and Engineering, Massachusetts Institute of Technology, 60 Vassar Street, Cambridge, MA, 02139, USA

4:05: 4B.2 **Effects of Ambient Conditions in Thermal Treatment for Ge(001) Surfaces on Ge MIS Interface Properties**, Noriyuki Taoka[1]; Keiji Ikeda[2]; Yoshimi Yamashita[2]; Naoharu Sugiyama[2]; Shin-ichi Takagi[1],[3]; [1]MIRAI-ASRC, AIST Tsukuba West 7 ,16-1, Onogawa, Tsukuba 305-8569, Japan; [2]MIRAI-ASET, AIST Tsukuba West 7, 16-1, Onogawa, Tsukuba, 305-8569 Japan; [3]The University of Tokyo, 7-3-1 Hongo, Bunkyo-Ku, Tokyo, 113-8656, Japan

4:20: 4B.3 **Ge nanocrystals metal-oxide-semiconductor capacitors with Ge nanocrystals formed by oxidation of poly-$Si_{0.88}Ge_{0.12}$**, J. H. Wu; P.W. Li; Dept of Electrical Engineering, National Central University, ChungLi, 32001 Taiwan ROC

4:35: 4B.4 **Thin Germanium-Carbon Layers on Silicon for Metal-Oxide-Semiconductor Devices**, David Q Kelly[1]; Isaac Wiedmann[1]; Domingo I Garcia Gutierrez[2]; Miguel Jose Yacaman2; Sanjay K Banerjee[1]; [1] Microelectronics Research Center, UT-Austin, 10100 Burnet Road, Bldg. 160, Austin, TX, 78758, USA, [2]Dept. of Chemical Engineering, UT-Austin; 1 University Station MS C0400, Austin, TX 78712 USA

Session 5: Poster Session/Reception
5:30 PM – 7:45 PM, Genomics Institute Lobby

5P.1 **Fabrication of Ge-dots/Si Multilayered Structures by Combination of Low-pressure CVD and Ni-induced Lateral Crystallization**, Y. Shi; B. Yan; L. Pu; K.J. Zhang: J.M. Zhu; G.B.Ma; P. Han; R. Zhang; Y.D. Zheng; Key Laboratory of Photonic and Electronic Materials, Department of Physics, Nanjing University, Nanjing, 210093, China

5P.2 **Proton Radiation Tolerance of SiGe Power HBTs**, Ningyue Jiang[1]; Zhenqiang Ma[1]; Pingxi Ma[2]; Marco Racanelli[2]; [1] Dept. of Electrical and Computer Engineering, University of Wisconsin-Madison, WI 53706 USA; [2] Jazz Semiconductor, Inc. USA

5P.3 **SiGe:C Epi processes with improved robustness against uncontrolled oxygen incorporation**, Roger Loo[1]; Tom Janssens[1]; Michael Pikulin[2]; Gary Miller[2]; [1] IMEC, Kapeldreef 75, Leuven (Heverlee), 3001, Belgium; [2] Voltaix Inc, 197 Meister Avenue, North Branch, NJ, 08876, USA

5P.4 **Impact of SiN on Performance in Novel CMOS Architecture Using Substrate Strained-SiGe and Mechanical strained-Si Technology**, Yu Min Lin; San Lein Wu[1]; Shoou Jinn Chang[1]; Pang Shiu Chen[2]; Chee Wee Liu[3]; Institute of Microelectronics and Dept. of Electronics

Engineering, National Cheung Kung University, Tainan, Taiwan, R.O.C.; [1 Dept]. of Electronics Engineering, Cheng Shiu University, Kaohsiung, Taiwan; [2] Dept. of Materials Science and Engineering, Ming Shin University of Science and Technology, Taiwan, R.O.C. [3] Dept. of Electrical Engineering, National Taiwan University, Taiwan, R.O.C.

5P.5 **Strained-Si nMOSFETs with Ni Silicide**, Yen Ping Wang[1]; San Lein Wu[2]; Shoou Jinn Chang[1]; [1] Institute of Microelectronics and Dept. of Electronic Engineering, National Cheung Kung University, Tainan, Taiwan, R.O.C; [.2]Dept. of Electronics Engineering, Cheng Shiu University, 840, Sheng Ching Rd., Neau-song, Kaohsiung, Taiwan 833

5P.6 **Tradeoff between Short Channel Effect and Mobility in Strained-Si nMOSFETs**, Yen Ping Wang[1]; San Lein Wu[2]; Shoou Jinn Chang[1]; [1] Institute of Microelectronics and Dept. of Electronic Engineering, National Cheung Kung University, Tainan, Taiwan, R.O.C; [.2] Dept. of Electronics Engineering, Cheng Shiu University, 840, Sheng Ching Rd., Neau-song, Kaohsiung, Taiwan 833

5P.7 **Room Temperature Steady-State and Transient Carrier Transport Properties of Germanium Single Electron/Hole Transistors**, W. T. Lai; Pei-Wen Li; Ming-Ting D Kuo; Dept. of Electrical Engineering, National Central University, ChungLi, Taiwan, 32001 R.O.C

5P.8 **A Tensorial High-Field Electron Mobility Model for Strained Silicon**, Siddhartha Dhar[1]; Hans Kosina[1]; Gerhard Karlowatz[1]; Enzo Ungersboeck[1]; Tibor Grasser[2]; Siegfried Selberherr[1]; [1] Institute for Microelectronics, Technical University Vienna, Gusshausstrasse 27-29/E360, 1040,Vienna, Austria; [2] Christian Doppler Laboratory for TCAD in Microelectronics, Vienna, Austria

5P.9 **Simulations of non-uniform, non-linear collector doping profiles for SiGe HBT's**, Edward Preisler; Will Cai; Jie Zheng; Marco Racanelli; Jazz Semiconductor, 4321 Jamboree Rd., Newport beach, CA 92660 USA

5P.10 **Determination of the surface segregation ratio of P in Si(100) during solid-source molecular beam epitaxial growth**, Phillip E Thompson; Glenn G Jernigan; Code 6812, Electronics Science and Technology Division, Naval Research Laboratory, Washington, DC 20375, USA

5P.11 **Thermoelectric Temperature Sensors Based on Si-Ge Whiskers**, A.A. Druzhinin; Ihor P Ostrovskii; Iu.R. Kogut; Lviv Polytechnic National University, 1 Kotlyarevskii St., 79013, Lviv, Ukraine

5P.12 **Effect of C incorporation on the growth kinetics of $Si_{1-x-y}Ge_xC_y$ layers**, Hyun-Woo Kim[1]; Suk Choi[1]; Sukwoon Hong[1]; Hye Kyung Jung[1]; Gun-Do Lee[1]; Chang Soo Kim[2]; Euijoon Yoon[1]; [1]School of Materials Science and Engineering, Seoul National University, San 56-1, Shillim-dong, Kwanak-gu, Seoul 151-744, Korea; [2] Materials Evaluation Center, Korea Research Institute of Standards and Science, Daejeon, 305-600, Korea

5P.13 **Strained Silicon on Insulator (SSOI) by Wafer Bonding**, Manfred Reiche[1]; Inout Radu[1]; Allistair Hoy[2]; Robert Harper[2]; [1] Max-Planck of Microstructure Physics, Weinberg 2, D-06120, Halle, Germany; [2] IQE Silicon Compounds, Beech House, Cypress Drive, St. Mellons, Cardiff CF3 OLW, United Kingdom

5P.14 **Growth of Strain-relaxed $Si_{1-y}C_y$ Films with Step Carbon Composition By Gas Source MBE**, Hanae Ishihara[1]; Masahiko Murano[1]; Akira Yamada[2]; Makoto Konagai[1]; [1] Dept. of Physical Electronics, Tokyo Institute of Technology, [2] Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, 2-12-1-S9-9, O-okayama, Meguro-ku, Tokyo, 152-8552, Japan

5P.15 **Effects of Mechanical Uniaxial Stress on SiGe HBT Characteristics**, Tzu-Juei Wang[1], Hung-Wei Chen[2]; Chih-Hsin Ko[2]; John Yeh[2]; Ping-Chun Yeh[2]; Shoou-Jinn Chang[1]; San Lein Wu[3]; Wen-Chin Lee[2]; Denny D. Tang[2], [1] Institute of Microelectronics and Dept. of Electrical Engineering, National Cheng Kung University, No.1 Ta-Hsuch Road, Tainan 701, Taiwan, R.O.C.; [2] Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan, R.O.C.; [3] Department of Electronics Engineering, Cheng Shiu University, 840, Sheng Ching Rd. Neau-song, Kauhsiung, Taiwan 833

5P.16 **The Interface Properties of SiO_2/Strained-Si with Carbon Incorporation Surface Channel MOSFETs**, Min Hung Lee[1]; S. T. Chang[2]; S. Maikap[3]; C.-Y. Yu[4]; C. W. Liu[4]; [1] Display Technology Center (DTC), Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan; [2] Dept. of Electrical Engineering, National Chung Hsing Univ., Taichung, Taiwan, [3] Electronics Research and Service Organization (ERSO), ITRI, Hsinchu, Taiwan; [4] Dept. of Electrical Engineering, National Taiwan University, Taipei, Taiwan

5P.17 **Optical properties, elasto-optical effects, and critical-point parameters of biaxially stressed**
$Si_{1-y}C_y$ alloys on Si (001), Stefan Zollner[1]; Victor H Vartanian[1]; J. P Liu[2]; Peter Zaumseil[3]; H. J Osten[4]; Alex A Demkov[5]; Bich-Yen Nguyen[1]; [1] Freescale Semiconductor, Inc., MD TX11, 3501 Ed Bluestein Blvd., Austin, TX, 78721, USA; [2] Chartered Semiconductor Manufacturing Ltd., Technology Development, Singapore 738406; [3] IHP- Microelectronics, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany; [4] Inst. of Electronic Materials and Devices, University of Hannover, Appelstr. 11a, D-30167, Hannover, Germany; [5] Dept. of Physics, University of Texas at Austin, Austin, TX, 78712 USA

5P.18 **A study of boron concentration uniformity in selective epitaxial growth for SiGe HBT**, S. Eguchi[1]; I. Miyashita[1]; Y. Kagotoshi[1]; H. Toyoda[2]; A. Kanai[1]; N. Machida[1]; [1] Renesas Technology Corp., 111 Nishiyokote, Takasaki, 370-0021, Japan; [2] Renesas Eastern Japan Semiconductors Inc., 1-1 Nishiyokote, Takasaki 370-0021, Japan

5P.19 **Strain and hole-density dependence of hole mobility in strained-Ge modulation-doped structures**, Kentarou Sawano[1]; Hikaru Satoh[1]; Yugo Kunishi[1]; Kiyokazu Nakagawa[2]; Yasuhiro Shiraki[1]; [1] Research Center for Silicon Nano-Science, Advanced Research Laboratories, Musashi Institute of Technology, 8-15-1 Todoroki, Setagaya-ku, Tokyo, 158-0082, Japan; [2] Center for Crystal Science and Technology, University of Yamanashi, 7 Miyamai-cho, Kofu 400-0021, Japan

5P.20 **High Temperature Growth of Very High Ge Content SiGe Virtual Substrates**, Jean-Michel HARTMANN; CEA-LETI, CEA-Grenoble, 17, Rue des Martyrs, Grenoble, 38054, FRANCE;

5P.21 **Growth and structure evaluation of strain-relaxed $Ge_{1-x}Sn_x$ buffer layers on virtual Ge(001) substrates**, Shotaro Takeuchi[1]; Akira Sakai[1]; Koji Yamamoto[1]; Osamu Nakatsuka[2]; Masaki Ogawa[3]; Shigeaki Zaima[1]; [1] Department of Crystalline Materials Science, Nagoya

University, Graduate School of Engineering, Japan; [2] Eco Topia Science Institute, Nagoya University; [3] Center for Cooperative Research in Advanced Science and Technology, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan

5P.22 **Enhancement of Hole Mobility and Carrier Density in Ge Quantum Well SiGe Heterostructure via Implementation of Double-Sides Doping**, Maksym Myronov; Kentarou Sawano; Yasuhiro Shiraki; Research Center for Silicon Nano-Science, Advanced Research Laboratories, Musashi Institute of Technology, 8-15-1 Todoroki Setagaya-ku, 158-0082, Tokyo, Japan

5P.23 **The Influence of the Collector Design on the f_{max} vs. f_t characteristics for Different Types of Si-based RF Bipolar Transistors**, Christian Schippel[1]; Frank Schwierz[1]; Jun Fu[2]; [1] Department for Solid State Electronics, Technical University Ilmenau, PF 100565, 98684, Ilmenau, Germany; [2] X-FAB Semiconductor Foundries AG, Haarbergstrasse 67, 99097 Erfurt, Germany

5P.24 **Carbon Doping Effect on Strain Relaxation during $Si_{1-x-y}Ge_xC_y$ Epitaxial Growth on Si(100) at 500 ^oC**, Hiroaki Nitta; Masao Sakuraba; Junichi Murota; Res. Inst. Electr. Comm., Tohoku Univ., 2-1-1 Katahira, Aoba-ku, Sendai, 980-8577, Japan

5P.25 **Hole Tunneling Properties in Resonant Tunneling Diodes with Si/Strained $Si_{0.8}Ge_{0.2}$ Heterostructures Grown on Si(100) by Low-Temperature Ultraclean LPCVD**, Ryota Ito; Masao Sakuraba; Junichi Murota; Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai, 980-8577, Japan

5P.26 **Epitaxial Growth of Highly Strained Si on Relaxed Ge/Si(100) Using ECR Plasma CVD without Substrate Heating**, Katsutoshi Sugawara; Masao Sakuraba; Junichi Murota; Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai, 980-8577, Japan

5P.27 **Epitaxial Growth of P Atomic Layer Doped Si Film by Alternate Surface Reaction of PH_3 and Si_2H_6 on Strained $Si_{1-x}Ge_x$/Si(100) in Ultraclean Low Pressure CVD**, Yohei Chiba; Masao Sakuraba; Junichi Murota; Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai, 980-8577, Japan

5P.28 **Formation of high quality strained-Si / strained-SiGe layers grown on relaxed SiGe virtual substrates for advanced CMOS application**, In-Kyum Kim; Suk-june Kang; Hyung-sang Yuk; Dong-kun Lee; Bo-young Lee; R&D Center, LG Siltron Inc., 283, Imsoo-dong, Gumi, Gyeong-buk, 730-724, Korea

5P.29 **Investigation of Geometry Scaling Effect on Si BJT and SiGe HBT fabricated on SOI Substrates**, Shu-Tong Chang[1]; S.H. Liao[2]; C.Y. Lin[2]; [1] Dept. of Electrical Engineering, National Chung Hsing University, Tai-Chung, Taiwan, R.O.C.; [2] Dept. of Physics, National Chung Hsing University, Tai-chung, Taiwan, R.O.C.

5P.30 **Study of Relaxation of Strain in Patterned Structures using X-Ray Diffraction Technique**, Aaliya Rehman Khan[1]; J. Stangl[1]; G.Bauer[1]; D. Buca[2]; B. Hollander[2]; H. Trinkaus[2]; S. Mantl[2]; R. Loo[3]; M. Caymax[3]; [1] Institute for Semiconductor Physics, JKU, Linz, Austria; [2] Center

of Nanoelectronic Systems for Information Technology, Forschungzentrum Julich GmbH, D-52425 Julich, Germany; [3] IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

5P.31 **Selective Epitaxial Growth of n-type Doped SiGe-structures with LPCVD**, Markus W Schindler[1]; Mathias Born[1]; Oliver Senftleben[1]; Ignaz Eisele[1]; William Taylor[2]; [1] Institute of Physics, University of the German Armed Forces Munich, 85577 Neubiberg, Germany; [2] Freescale Semiconductor Inc., 3501 Ed Bluestein Boulevard, Austin, TX, 78721 USA

5P.32 **Physical and Electrical Characteristics of Metal-Oxide-Semiconductor Capacitor Containing Germanium Nanocrystals**, K H Chiang[1]; S W Lu[1]; Y H Peng[1]; P S Chen[2]; C H Kuan[1]; [1] Dept. of Electrical Engineering and Graduate Studies of Electronics Engineering, National Taiwan University, No.1, Sec. 4, Roosevelt Road, Taipei, 10617; [2] Department of Materials Science and Engineering, Ming Hsin University of Science and Technology, No. 1 Hsin Hsin Road Hsin Feng, Hsin Chu, Taiwan

5P.33 **Theory of X-ray Diffraction from Partially Relaxed SiGe/Si Layers**, Helmut Trinkaus[1]; Dan Buca[2]; Bernd Holländer[2]; Siegfried Mantl[2]; Aaliya Rehman Khan[3]; G. Bauer[3]; [1] Institut fur Festkorperforschung, Forschungszentrum Juelich, D-52428, Juelich, Germany; [2] Center of Nanoelectronic Systems for Information Technology, Forschungzentrum Julich GmbH, D-52425 Julich, Germany; [3] Institute for Semiconductor Physics, JKU, Linz, Austria

5P.34 **Study of surface roughness and dislocation generation in strained Si Layers grown on thin strain-relaxed buffers for high performance MOSFETs**, Enrique Escobedo-Cousin[1]; Sarah H Olsen[1]; Steve J Bull[1]; Anthony G O'Neill[1]; Howard Coulson[2]; Cor Claeys[3]; Roger Loo[3]; Romain Delhougne[3]; Matty Caymax[3]; [1] University of Newcastle, UK; [2] Atmel North Tyneside, UK; [3] IMEC, Leuven, Belgium

5P.35 **Analysis of Electron Mobility in Relaxed and Strained $Si_{1-x}C_x$ alloys**, Shu-Tong Chang[1]; C.Y. Lin[2]; S.H. Liao[1]; [1] Dept. of Electrical Engineering, National Chung Hsing University, , Tai-Chung, Taiwan R.O.C.; [2] Dept. of Physics, National Chung Hsing University, Tai-Chung, Taiwan R.O.C.

5P.36 **Characteristics of Superlattice LED with a $Si_{0.8}Ge_{0.2}$ or Si Capped Layer at Room Temperature**, Y. H. Peng[1]; H.R. Li[1]; P.S. Chen[2]; Y.W. Suen[3]; C.H. Kuan[1]; S.C. Lee[1]; 1 Graduate Institute of Electronics Engineering, National Taiwan University, No.1, Sec. 4, Roosevelt Road, Taipei, Taiwan 106, R. O. C.; [2] Dept. of Materials Science and Engineering, Ming Hsin University of Science and Technology, No.1 Hsin Hsin Road, Hsin Feng, Hsin Chu, Taiwan, R.O.C.; [3] Dept. of Physics, National Chung-Hsing University, Taichung, Taiwan, R.O.C.

5P.37 **A High Performance Photodetector in Standard SiGe BiCMOS Technology**, Kuang-Sheng Lai; Ji-Chen Huang; Klaus Y.-J. Hsu; Institute of Electronics Engineering, National Tsing Hua University, 101 Sec 2, Kuang Fu Road, Hsingchu, 30055, Taiwan R.O.C.

5P.38 **A Study of Low Energy Phosphorus Implantation and Annealing in Si:C Epitaxial Films**, Zhiyuan Ye; Yihwan Kim; Ali Zojaji; Errol Sanchez; Yonah Cho; Matthew Castle; Majeed A Foad; Applied Materials, 974 East Arques, M/S 81288, Sunnyvale, CA, 94085, USA

5P.39 **Current Gain of SiGe HBTs Under High Base Doping Concentrations**, Ningyue Jiang; Zhenqiang Ma; Department of Electrical and Computer Engineering, University of Wisconsin,

Madison, WI, 53706, USA

5P.40 **Low-temperature Pre-treatments in Vertical Epitaxial Reactor with Improved Vacuum Load-Lock Chamber**, Jie Wang; Yasuhiro Inokuchi; Yasuo Kunii; Hitachi Kokusai Electric Inc., 2-1 Yasuuchi, Yatsuo-machi, Toyama, 939-2393, Japan

5P.41 **Growth of Ultra-uniform B-doped Si/SiGe Multiple Quantum Wells by RTCVD for Mid-IR Applications**, W. Zheng[1]; J. C. Sturm[1]; C. Gmachl[1]; T. Buyuklimanli[2]; J. Marino[2]; M. S. Denker[2]; J. T. Mayer[2]; [1] Princeton Institute for the Science and Technology of Materials, Dept. of Electrical Engineering, Princeton University, Princeton, NJ, 08544, USA; [2] Evans Analytical Group, 104 Windsor Center, Suite 101, East Windsor, NJ, 08520, USA

5P.42 **Bound-to-Continuum Quantum Cascade Emitters for Terahertz Emission**, Douglas J Paul[1]; Paul Townsend[1]; Stephen A Lynch[1]; Ming Zhao[2]; Wei-Xin Ni[2]; Jing Zhang[3]; [1] University of Cambridge, Cavendish Laboratory, Madingley Road, Cambridge, CB3 0HE, U.K.; [2] University of Linkoping, Department of Physics and Measurement Technology, Linkoping, S-58183, Sweden; [3] Imperial College London, Department of Physics, Blacket Laboratory, London, SW7 2BW, U.K.

5P.43 **Integration of selective SiGe epitaxy for source/drain application in MOSFETs**, Henry H Radamson; Julius Hållstedt; Mikael Östling; School of Information and Communication, Royal Institute of Technology (KTH), Isafjordsg. 22-26, Electrum 229, 16640, Kista, Sweden

5P.44 **Xenon Difluoride dry etching of Si, SiGe alloy and Ge**, Guangchi Xuan[1]; Thomas N Adam[1*]; John Suehle[2]; Eugene Fitzgerald[3]; Pengcheng Lv[1]; Nathan Sustersic[1]; Matthew Coppinger[1]; James Kolodzey[1]; [1] University of Delaware, 140 Evans Hall (ECE Dept.), Newark, DE, 19716, USA; [2] National Institute of Standards and technology, Gaithersburg, Maryland 20899; [3] Materials Science and Engineering Dept., MIT, Cambridge, MA, USA; [1*] now with IBM Corp., 1101 Kitchawan Road, Route 134/P.O. Box 218, Yorktown, NY 10598 USA

5P.45 **Effective Mass Measurement: Influence of Hole Band Nonparabolicity in SiGe/Ge Quantum Wells**, Benjamin Rössner[1]; Hans von Känel[1,2]; Daniel Chrastina[2]; Giovanni Isella[2]; Betram Batlogg[1]; [1] Laboratory for Solid State Physics, ETH Zürich, CH-8093 Zürich, Switzerland; [2] :L-NESS Dipartimento di Fisica, Polo Regionale di Como del Politecnico di Milano, I-22100 Como, Italy

5P.46 **Influence of Collector Design on the SiGe HBT's Quasi-Saturation Characteristics**, Will Cai; Jie Zheng; Ed Preisler; Paul Hurwitz; Marco Racanelli; Jazz Semiconductor, 4321 Jamboree Rd., Newport Beach, CA, 92660, USA

5P.47 **Highly tensile strained Silicon Carbon Phosphorus alloys epitaxially grown into recessed source drain areas of NMOS devices**, Matthias Bauer[1]; Vladimir Machkauostan[2]; Chantal Arena[1]; [1] ASM America, 3440 East University Drive, Phoenix, AZ 85034, USA; [2] ASM Belgium, Kapeldreef 75, B-3001 Leuven, Belgium

5P.48 **Systemic study of thick strained silicon NMOSFETs for digital applications**, J.G. Fiorenza[1]; P. Kohli[3]; S.J. Kang[4]; M. Erdtmann[1]; M. Curtin[1]; S. Bengston[1]; K. Matthews[2]; B. Nguyen[2]; I.K. Kim[4]; H.S. Yuk[4]; D.K. Lee[4]; B.Y. Lee[4]; A. Lochtefeld[1]; R. Wise[3]; [1] AmberWave Systems Corporation, Salem, NH, USA; [2] Advanced Technology Development Facility, Austin,

TX, USA; [3] Silicon Technology Development, Texas Instruments, Dallas, TX, USA; [4] LG Siltron, Gumi, Korea

Session 6: Panel Discussion: *What's the next big thing for SiGe after strained Si and HBTs?*
8:00 PM – 9:30 PM, Friend 101

Tuesday, May 16, 2006

Registration and Breakfast
7:45 AM – 8:30 AM, Friend Center 113

Session 7: Invited: FET's and CMOS
8:30 AM – 10:30 AM, Friend 101

8:30: 7.1 **High mobility nano-scaled CMOS: some opportunities and challenges**, Thomas Ernst[1]; Francois Andrieu[1]; Olivier Weber[1,2]; Cecilia Dupré[1,2]; Olivier Faynot[1]; Frédérique Ducroquet[2,1]; Laurent Clavelier[1]; Jean-Michel Hartmann[1]; Sylvain Barraud[1]; Gérard Ghibaudo[2]; Simon Deleonibus[1]; [1] CEA/DRT-LETI, 17 Rue des Martyrs, 38054 Grenoble Cedex 9, France; [2] IMEP, UMR CNRS, ENSERG, BP 257, 38016 Grenoble, France

9:00: 7.2 **Strained and relaxed SiGe for high-mobility MOSFETs**, Minjoo L Lee; Dimitri Antoniadis; Eugene A Fitzgerald; MIT, 77 Massachusetts Ave., 13-4154, Cambridge, MA, 02139, USA

9:30: 7.3 **Strained-SOI/SGOI Dual Channel CMOS Technology Based on Ge Condensation Technique**, Tsutomu Tezuka[1]; Shu Nakaharai[1]; Yoshihiko Moriyama[1]; Norio Hirashita[1]; Eiji Toyoda[2]; Toshinori Numata[1]; Toshifumi Irisawa[1]; Koji Usuda[1]; Naoharu Sugiyama[1]; Tomohisa Mizuno[3,4]; Shin-ichi Takagi[3,5]; [1] MIRAI-ASET, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 212-8582, Japan; [2] Toshiba Ceramics , Japan; [3] MIRAI-AIST, Japan; [4] Kanagawa Univ.; [5] Univ. of Tokyo, Japan

10:00: 7.4 **Strained SOI/GOI**, M Kennard[1]; [1] SOITEC, Bernin, France;

Break
10:30 AM – 10:50 AM, Friend 113

[Parallel Session]
Session 8A: Strained Si FET's/Selective Epitaxy
10:50 AM – 12:05 PM, Friend 101

10:50: 8A.1 **Effective Surface Treatments for Selective Epitaxial SiGe Growth in Locally Strained pMOSFETs**, Chin-I Liao[1]; Yi-Cheng Chen[1]; Po-Lun Cheng[1]; Hsiang-Ying Wang[1]; Chin-Cheng Chien[1]; Chan-Lon Yang[1]; K T Huang[1]; S F Tzou[1]; Jinsong Tang[2]; Rohini Kodali[2]; Lori Washington[2]; Vincent C Chang[2]; Tony Fu[2]; Yonah Cho[2]; [1] United Microelectronics Corp., No 18, Nanke 2nd Rd. Tainan Science Park, Sinshih Township, Tainan County, 741, Taiwan R.O.C.; [2] Applied Materials, 974 E. Arques Avenue, Sunnyvale, CA, 94086, USA

11:05: 8A.2 **Selective Epitaxial Si/SiGe for V_T Shift Adjustment in High k pMOS Devices**, Roger Loo[1]; Haruyuki Sorada[2]; Akira Inoue[2]; Byeong Chan Lee[3]; Sangjin Hyun[3]; Guilherme Lujan[1*]; Thomas Y. Hoffmann[1]; Matty Caymax[1]; [1]IMEC, Kapeldreef 75,B-3001 Leuven (Heverlee), Belgium; [2]assigned to IMEC from Matsushita Electric Industrial Co., Ltd., 3-1-1 Yagumo-naka-machi, Moriguchi, Osaka, 570-8501, Japan; [3]assigned to IMEC from Samsung Electronics Co., San#24 Nongseo-Ri, Giheung-Eup, Yongin-City, Gyeonggi-Do, Korea 449-711 *current address: Austriamicrosystems AG, Schloss Premstatten, A 8141, Austria

11:20: 8A.3 **High Density Planes Deposition Kinetics and Facets Propagation in Silicon Selective Epitaxial Growth**, N. Loubet; A. Talbot; D. Dutartre; STMicroelectronics, 850 rue Jen Monnet, 38926 Crolles Cedex, France

11:35: 8A.4 **Growth kinetics of Si and SiGe on Si(100), Si(110) and Si(111) surfaces**, J. M. Hartmann; M. Burdin; G. Rolland; T. Billon; CEA-DRT, LETI/D2NT & DPTS, CEA/GRE – 17, Avenue des Martyrs 38054 Grenoble Cedex 9, France

11:50: 8A.5 **Flexible Thin-film Transistors on Strained Si/SiGe Membranes**, Hao-Chih Yuan[1]; Guogong Wang[1]; Michelle M Roberts[2]; Donald E Savage[2]; Max G Lagally[2]; Zhenqiang Ma[1]; [1]Dept. of Electrical and Computer Engineering; [2]Dept. of Materials Science and Engineering, University of Wisconsin-Madison, 1415 Engineering Dr., Madison, WI, 53706, USA

[Parallel Session]
Session 8B: Heterostructure Growth and Novel Characterization
10:50 AM – 12:05 PM, CS104

10:50: 8B.1 **Selective MBE of High-Quality Ge on Si Covered with SiO_2**, Qiming Li[1]; Darin Leonhardt[1]; Joshua L Krauss[1]; Stephen Hersee[2]; Sang M Han[1]; [1]Dept. of Chemical & Nuclear Engineering, University of New Mexico, 209 Farris Engineering Center, Albuquerque, NM 87131, USA [2]Center for High Technology Materials, University of New Mexico, 1313 Goddard SE, Albuquerque, NM 87106, USA

11:05: 8B.2 **High Growth Rate of Epitaxial Silicon-Carbon Alloys by High-Order Silane Precursor and Chemical Vapor Deposition**, K. Chung[1]; J.C. Sturm[1]; E. Sanchez[2]; S. Kuppuroa[2]; [1] Princeton Institute for the Science and Technology of Materials (PRISM) and Dept. of Electrical Engineering, Princeton University, Princeton, NJ, 08544, USA; [2]Applied Materials, 3050 Bowers Avenue, Santa Clara, CA, 95054 USA

11:20: 8B.3 **Three-dimensional characterization of SiGe structures with a laser assisted local electrode atom probe**, Keith Thompson; David J Larson; Joseph H Bunton; Thomas F Kelly; Imago Scientific Instruments, 6300 Enterprise Ln. Suite 100, Madison, WI, 53719, USA

11:35: 8B.4 **Characterization of a SiGe layer after isotropic etching of surrounding Si.**, Stephan Borel[1]; Véronique Caubet[2]; Dominique Lafond[1]; Olivier Kermarrec[2]; Yves Campidelli[2]; [1]CEA/Leti, 17 Rue des Martyr, 38054 Grenoble Cedex 9, France; [2] ST Microelectronics, 850 Rue Jean Monnet, 38926 Crolles, France

11:50: 8B.5 **Intense photoluminescence from Ge(Si) self-assembled islands embedded in a tensile-strained Si layer**, A.V, Novikov[1]; M.V. Shaleev[1]; A. N. Yablonskiy[1]; O. A. Kuznetsov[2];

Y. N. Drozdov[1]; D. N. Lobanov[1]; Z.F. Krasilnik[1]; [1]Institute for Physics of Microstructures, RAS, 603950, Nizhny Novgorod, GSP-105, Russia; [2]Physical-Technical Research Institute, Nizhny Novgorod State University, 603950, Nizhny Novgorod, Russia

Session 9: Poster Session and Lunch
12:05 PM – 2:00 PM, Friend Center 113

Session 10: Invited: Quantum Devices and Novel Structures
2:00 PM – 3:30 PM, Friend 101

2:00: 10.1 **SiGe Quantum Cascade Structures: Physics, Growth and Technology**, Detlev Grützmacher[1]; S. Tsujino[1]; G. Mussler1; V. Shushunova[1]; M. Scheinert[1]; E. Müller[1]; N. Demarina[1]; H. Sigg[1]; J. Faist[2]; O. Kerrmarrec[3]; [1] Laboratory for Micro- and Nanotechnology, Paul Scherrer Institut, CH-5232, Villigen-PSI, Switzerland; [2] Institute of Physics, University of Nuechatel, 1 A.-L. Breguet, CH-2000 Switzerland; [3] STMicroelectronics, Crolles, F-38926 France

2:30: 10.2 **SiGe: Materials and Devices for Quantum Computing,** Mark A. Eriksson; University of Wisconsin-Madison, 1150 University Ave., Madison, WI, 53706, USA

3:00: 10.3 **SiGe/Si "Micro-Origami" epitaxial MEMS device on SOI substrate**, Takashi Tokuda; Masahiro Nunoshita; Jun Ohta; Graduate School of Materials Science, Nara Institute of Science and Technology, Takayama 8916-5, Ikoma, Nara, 630-0101, Japan

Break
3:30 PM – 3:45 PM, Friend 113

[Parallel Session]
Session 11A: Virtual Substrates
3:45 PM – 5:15 PM, Friend 101

3:45: 11A.1 **Formation of SGOI structures with low dislocation density by two step oxidation and condensation method**, N. Sugiyama[1]; S. Nakaharai[1]; N. Hirashita[1]; T. Tezuka[1]; Y. Moriyama[1]; K. Usuda[1]; S. Takagi[2,3]; [1] MIRAI-ASET; [2] MIRAI-AIST, University of Tokyo, 1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki, Japan

4:00: 11A.2 **Fabrication of SiGe-On-Insulator by Improved Ge condensation technique**, J.F. Damlencourt[1]; B. Vincent[1]; P. Riyallin[1] P. Holliger[1], D. Rouchon[1], E. Nolot[1], C. Licitra[1], Y. Morand[2], L. lavelier[1] ; T. Billon[1]; [1]CEA-DRT-LETI – CEA/GRE, 17 avenue des martyrs, Grenoble Cedex 9, France;
[2] ST Microelectronics, 12 rue Jules Horowitz, 38000 Grenoble, France

4:15: 11A.3 **Single Wafer sSOI by SIMOX**, J. P de Souza; S. W Bedell; H. J. Hovel; K. Fogel; A. Reznicek; D. K Sadana; IBM, T. J. Watson Research Center, 1101 Kitchawan Rd / Rte 134, Yorktown Heights, NY, 10598; USA

4:30: 11A.4 **Strain Relaxation in Strained-Si Layer on SiGe-on-Insulator Substrate**, Norio Hirashita[1]; Yoshihiko Moriyama[1]; Eiji Toyoda[2]; Naoharu Sugiyama[1]; Shin-ichi Takagi[3]; [1]MIRAI-ASET, 1, Komukai Toshiba-cho, Saiwaiku, Kawasaki, 212-8216, Japan; [2] Toshiba Ceramics Co., Ltd., Seirou-machi, Kitakanbara-gun, Nigata, 957-0197, Japan; [3]MIRAI-AIST, Tsukuba, 305-8569,

Japan

4:45: 11A.5 **Generation of Crystal Defects in Ge-on-Insulator (GOI) Layers in Ge-condensation Process**, S. Nakaharai[1]; T. Tezuka[1]; N. Hirashita[1]; E. Toyoda[2]; Y. Moriyama[1]; N. Sugiyama1; S. Takagi[3],[4]; [1] MIRAI-ASET, 1, Komukai-toshiba-cho, Saiwai-ku, Kawasaki, 212-8582, Japan; [2] Toshiba Ceramics, 6-864-5 Higashikou, Seirou-Machi, Kitakanbara-gun, 957-0197, Japan; [3] MIRAI(ASET), 1, Komukai-toshiba-cho, Saiwai-ku, Kawasaki, 212-8582; [4]University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan

5:00: 11A.6 **Reducing threading dislocation densities in SiGe mismatched layers by controlling strain rate and surface roughness**, Saurabh Gupta; Yu Bai; David M Isaacson; Eugene A Fitzgerald; Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA, 02139, USA

[Parallel Session]
Session 11B: Novel/Quantum Devices
3:45 PM – 5:15 PM, CS 104

3:45: 11B.1 **Direct Measurement of HH2-HH1 Intersubband Lifetimes in SiGe Quantum Cascade Structures**, P. Rauter[1]; T. Fromherz[1]; G. Bauer[1]; N.Q. Vinh[2], P.J. Phillps[3], C.R. Pidgeon[3], B.N. Murdin[4], L. Diehl[6], G. Dehlinger[5], D. Grutzmacher[5]; [1]Institute for Semiconductor and Solid State Physics, Johannes-Kepler-University Linz, Austria, [2]FOM Institute for Plasma Physics Rijnhuizen, Nieuwegein, Netherlands, [3]Heriot-Watt University, Edinburgh, UK, [4]University of Surrey, Guildford, UK, [5]Paul Scherrer Institut, Villingen, Switzerland, [6] Princeton University, USA

4:00: 11B.2 **Thermoelectric Power Generation using Large Area Si/SiGe pn-Junctions with varying Ge-content**, M. Wagner [1]; G. Span[2]; T. Grasser [1]; [1]Institute for Microelectronics, Gusshausstr. 27-29/E360, 1040 Vienna, Austria; [2] SAM – Span and Mayrhofer KEG, 6112 Wattens, Austria

4:15: 11B.3 **Lateral Quantum Dot in Si/SiGe realized by a Schottky Split-Gate Technique**, Thomas P Berer; Dietmar Pachinger; Georg Pillwein; Michael Mühlberger; Herbert Lichtenberger; Gerhard Brunthaler; Friedrich Schäffler; Institut fur Halbleiter-und Festkorperphysik, Johannes Kepler University, Altenbergerstrasse 69, A- 4040, Linz, Austria

4:30: 11B.4 **Investigation of upper and lower limits of carrier concentration for two-dimensional electron gas in strained silicon**, Jian Liu[1]; Bin Shi[1]; Keji Lai[2]; Tzu-Ming Lu[2]; Ya-Hong Xie[1]; Daniel C Tsui[2]; [1] Dept. of Materials Science and Engineering, University of California at Los Angeles, Box 951595, Los Angeles, California 90095-1595, USA; [2] Dept. of Electrical Engineering, Princeton University, Princeton, NJ, 08544 USA

4:45: 11B.5 **Electroluminescence from the Ge quantum dot metal-oxide-semiconductor tunneling diodes**, M. H. Liao[1]; T.-H Cheng[2]; T. C Chen[2]; C.-H Lai[1]; C.-H Lee[2]; C W Liu[1,2]; [1] Dept. of Electrical Engineering and Graduate Institute of Electro-Optical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. [2] Dept. of Electrical Engineering and Graduate Institute of Electronic Engineering, National Taiwan University, Taipei, Taiwan, R.O.C.

5:00: 11B.6 **Metal-insulator-metal photodetectors with Ge quantum dots formed by selective**

oxidation of single crystalline-$Si_{0.85}Ge_{0.15}$/Si-on-insulator, S. S. Tzeng; P.W. Li; W.M. Laio; W.T. Liah; Dept. of Electrical Engineering, National Central University, No.300, Chungda Rd., Taoyuan, Taiwan, R.O.C. 320

Conference Banquet: Reception
6:00 PM – 7:00 PM, Prospect House

Conference Banquet: Dinner
7:00 PM – 9:00 PM, Prospect House

Wednesday, May 17, 2006

Registration and Breakfast
7:45 AM – 8:30 AM, Friend Center 113

Session 12: Invited: HBT's, FET's, and CMOS
8:30 AM – 10:30 AM, Friend 101

8:30: 12.1 **SiGe BiCMOS Technologies for Improving Sensitivity and High-Speed Characteristics of the Communication LSIs**, Makoto Miura[1]; Hiromi Shimamoto[3]; Reiko Hayami[1]; Akihiro Kodama[3]; Tatsuya Tominari[2]; Takashi Hashimoto[2]; Katsuyoshi Washio[1]; [1] Central Research Laboratory, Hitachi, Ltd., Tokyo 185-8601, Japan; [2] Micro Device Division, Hitachi Ltd. [3] Renesas Northern Japan Semiconductor, Inc. Japan

9:00: 12.2 **High-Performance BiCMOS Technologies without Epitaxially-Buried Subcollectors and Deep Trenches**, Bernd Heinemann; R. Barth; D. Knoll H. Rücker; B. Tillack; W. Winkler; IHP, Im Technologiepark 25, Frankfurt (Oder), 15236, Germany

9:30: 12.3 **Control and characterization of strain in SiGe/Si heterostructures with engineered misfit dislocations**, Akira Sakai[1]; Noriyuki Taoka[1a]; Shogo Mochizuki[1]; Katsunori Yukawa[1]; Osamu Nakatsuka[2]; Shingo Takeda[3]; Shigeru Kimura[3,4]; Masaki Ogawa[5]; Shigeaki Zaima[1]; [1] Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan; [2] EcoTopia Science Institute, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan; [3] JASRI/Spring-8, Kouto, Mikazuki-cho, Sayo-gun, Hyogo 679-5198, Japan; [4] CREST, JST, Honmachi, Kawaguchi, Saitama 332-0012, Japan; [5] CCRAST, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan

10:00: 12.4 **Uniaxial and Biaxial Strain for CMOS Performance Enhancement**, Bich-Yen Nguyen; Debby Eades; Victor H Vartanian; Jon Cheek; Da Zhang; Bruce E White; Suresh Venkatesan; Aaron Thean; Paul A Grudowski; Ted R White; Stefan Zollner; David Theodore; Brian J Goolsby; Heather Desjardins; Lata Prabhu; Ricardo Garcia; John Hackenberg; Veer Dhandapani; Sharon Murphy; Raghaw S Rai; James R Conner; Patrick K Montgomery; Colita M Parker; Jill Hildreth; Ross E Noble; Mo Jahanbani; Freescale Semiconductor, 3501 Ed Bluestein Blvd., Mail Drop K10, Austin, TX, 78712, USA

Break
10:30 AM – 10:50 AM, Friend 113

[Parallel Session]
Session 13A: HBT Devices
10:50 AM – 11:55 AM, Friend 101

10:50: 13A.1 **Carbon effect on neutral base recombination in high-speed SiGeC HBTs**, Benoit Barbalat[1],[2]; Thierry Schwartzmann[1]; Pascal Chevalier[1]; Benoit Vandelle[1]; Laurent Rubaldo[1]; Fabienne Saguin[1]; Nicolas Zerounian[2]; Frédéric Aniel[2]; Alain Chantre[1]; [1] STMicroelectronics, 850 rue Jean Monnet, Crolles Cedex, 38926, France; [2] Institut d'Electronique Fondamentale, Bat. 220, Université Paris Sud 11, F-91405 Orsay Cedex, France

11:05: 13A.2 **Improved Carbon Incorporation in Selective Epitaxial Growth of SiGe:C for HBT Applications**, Florence Brossard; Benoît Vandelle; Pascal Chevalier; Didier Dutartre; STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, 38926, France

11:20: 13A.3 **Influence of lateral device scaling and airgap deep trench isolation on reliability performance of 200GHz SiGe:C HBTs**, Andreas Piontek[1]; Tony Vanhoucke[2]; Stefaan Van Huylenbroeck[1]; Li Jen Choi[1]; G.A.M. Hurkx[2]; E. Hijzen[2]; S. Decoutere[1]; [1] IMEC, Kapeldreef 75, Leuven, B-3001, Belgium; [2] Philips Research Leuven, Kapeldreef 75, Leuven, B-3001, Belgium

11:35: 13A.4 **Thermal Resistance of SiGe HBTs at High Power Densities**, Hui Li[1]; Zhenqiang Ma[1]; Pingxi Ma[2]; Marco Racanelli[2]; [1] Department of Electrical and Computer Engineering, University of Wisconsin-Madison, 1415 Engineering Drive, Madison, WI, 53705,USA [2] Jazz Semiconductor, Inc., Newport Beach, CA, 92660; [3] Jazz Semiconductor, Inc., Newport Beach, CA, 92660 USA

11:50: 13A.5 **On the Scaling of Emitter Stripes of SiGe Power HBTs**, Guogong Wang; Hao-Chih Yuan; Zhenqiang Ma; University of Wisconsin, 1415 Engineering Drive, Madison, WI, 53706 USA

[Parallel Session]
Session 13B: Relaxation of Patterned/Asymmetric Structures
10:50 AM – 11:55 AM, CS 104

10:50: 13B.1 **Characterization of in-plane strain relaxation in strained layers after mesa isolation using a newly developed plane-NBD method**, Koji Usuda[1]; Toshifumi Irisawa[1]; Toshinori Numata[1]; Norio Hirashita[1]; Shinichi Takagi[2]; [1] MIRAI-ASET; MIRAI-AIST; [2]University of Tokyo, Japan

11:05: 13B.2 **Fabrication and Characterization of Patterned Si/SiGe Lines with Asymmetric Biaxial Stress**, Dan M Buca[1]; Bernd Holländer[1]; Sebastian Feste[1]; Helmut Trinkaus[1]; Siegfried Mantl[1]; R. Loo[2]; Matty Caymax[2]; [1] Center for Nanoelectronic Systems for Information Technology, Forschungszentrum Juelich, 52428, Germany; [2] IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

11:20: 13B.3 **Dynamics of uniform Si/SiGe uniaxial strain generation on compliant insulation substrates**, Rebecca L Peterson; James C Sturm; Princeton Institute for the Science and Technology of Materials (PRISM) and Department of Electrical Engineering, Princeton University, 320 Bowen Hall, 70 Prospect Ave, Princeton, NJ, 08540, USA

11:35: 13B.4 **Strain Control and Electrical Properties of Stripe Patterned Si/$Si_{1-x}Ge_x$/Si(100) Heterostructures**, Jangwoong Uhm; Masao Sakuraba; Junichi Murota; Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai, 980-8577, Japan

11:50: 13B.5 **Strain relaxation of patterned Ge and SiGe layers on Si(001) substrates**, Shogo Mochizuki[1]; Akira Sakai[1]; Osamu Nakatsuka[2]; Hiroki Kondo[1]; Katsunori Yukawa[1]; Koji Izunome[3]; Takeshi Senda[3]; Eiji Toyoda[3]; Masaki Ogawa[4]; Shigeaki Zaima[1]; [1] Dept. of Crystalline Materials Science, Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan; [2] EcoTopia Science Institute, Nagoya University; [3] Toshiba Ceramics Co., Ltd., 6-861-5 Higashikou, Seirou-machi, Kitakanbara-gun, Niigata 957-0197, Japan; [4] CCRAST, Nagoya University, Furo-cho, Chikusa-Ku, Nagoya 464-8603 Japan

Lunch
12:05 PM – 1:30 PM, Friend Center 113

Session 14: Invited: HBT Circuits and Engineered Substrates
1:30 PM – 2:30 PM, Friend 101

1:30: 14.1 **Progress in SiGe Technology Toward Full Integrated mmWave ICs**, Brian Gaucher[1]; Scott K Reynolds[1]; Brian Floyd[1]; Ullrich Pfeiffer[1]; Troy Beukema[1]; Alvin Joseph[2]; Essam Mina[2]; Bradley Orner[2]; Richard Wachnick[3]; Keith Walter[3]; [1]IBM Research 1101 Kitchawan Rd./Rte.134, Yorktown Heights, NY, 10598, USA; [2] IBM S&TG, 1000 River St. Essex Junction, VT 05452 USA; [3] IBM S&TG, 2070 Rt. 52, M/S EM1, Hopewell Junction, NY 12533, USA

2:00: 14.2 **Enhancing CMOS Transistor Performance using Lattice-Mismatched Materials in Source/Drain Regions**, Yee-Chia Yeo; Dept. of Electrical and Computer Engineering, National University of Singapore, S117576, Singapore

Break
2:30 PM – 2:45 PM, Friend 113

[Parallel Session]
Session 15A: HBT Devices and Circuits
2:45 PM – 4:00 PM, Friend 101

2:45: 15A.1 **SiGe HBT design for CMOS compatible SOI**, Alain Chantre[1]; Grégory Avenier[1,2]; Pascal Chevalier[1]; Benoit Vandelle[1]; Fabienne Saguin[1]; Cristell Maneux[2]; Didier Dutartre[1]; Thomas Zimmer[2]; [1] STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France [2] Laboratoire de Microelectronique IXL, CNRS UMR 5818, Universite Bordeaux 1, F-33405, Talence, France

3:00: 15A.2 **SiGe HBT Linearity Comparison Between CE and CB Configurations**, Guoxuan Qin; Ningyue Jiang; Guogong Wang; Zhenqiang Ma; University of Wisconsin-Madison, Dept. of

Electrical and Computer Engineering, 1415 Engineering Drive, Madison, WI 53706 USA

3:15: 15A.3 **p-i-n Diodes for Monolithic Millimeter Wave BiCMOS Applications**, Bradley A Orner[1]; Qizhi Liu[1]; Jeffrey Johnson[1]; Robert Rassel[1]; Xuefeng Liu[1]; David Sheridan[1]; Alvin Joseph[1]; Brian Gaucher[2]; [1] IBM, Systems and Technology Group, 1000 River Road, Essex Junction, Vermont 05452 USA; [2] IBM, T.J. Watson Research Center, 1101 Kitchawan Ave., Yorktown Heights, NY 10598 USA

3:30: 15A.4 **SiGe Impulse Generator for Single-Band Ultra-Wideband Applications**, Jochen Dederer; Andreas Trasser; Hermann Schumacher; University of Ulm, Dept. of Electron Devices and Circuits, Albert-Einstein-Allee 45, 89069, Ulm, Germany

3:45: 15A.5 **X-band and K-band low-phase-noise VCOs using SiGe BiCMOS technology**, Jean-Guy Tartarin[1, 2]; King W. Wong[3]; Eric Tournier[1,2]; Olivier Llopis[2]; [1] Paul Sabatier University [2] LAAS-CNRS, 7 av. du Colonel Roche, 31.077, Toulouse cedex 4, FRANCE; [3] Institute of Microelectronics, 11 Science Park Road, Singapore Science Park II, Singapore, 117685

[Parallel Session]
Session 15B: Process Technology
2:45 PM – 4:00 PM, CS 104

2:45: 15B.1 **Surface Segregation and Electrical Studies of Heavily Arsenic and Phosphorus in situ Doped Epi and Poly Silicon.**, Gaël Borot[1]; Laurent Rubaldo[1]; Nicolas Breil[1]; Jumana Boussey[2]; Xavier Mescot[3]; Gérard Ghibaudo[3]; Didier Dutartrec[1]; [1] STMicroelectronics, 850, rue Jean Monnet, 38926 Crolles Cedex , France; [2] Laboratoire des Technologies de la Microelectronique, LTM-CNRS-CEA-LETI-D2NT; [3] Institut de Microelectronique, Electromagnetisme and Photonique (IMEP), ENSERG, France

3:00: 15B.2 **Phosphorus Segregation Control for SiGe:C Epitaxy**, Yuji Yamamoto; Klaus Köpke; Peter Zaumseil; Bernd Tillack; IHP, Im Technologiepark 25, Frankfurt (Oder), 15236, Germany

3:15: 15B.3 **Thermal Stability of strained-SOI (sSOI)**, Atsushi Fukumoto[1]; Kentaro Sawano[1]; Yusuke Hoshi[1]; Makoto Yoshimi[1,2]; Yasuhiro Shiraki[3]; [1] Musashi Institute of Technology, 8-15-1 Todoroki, Setagaya-ku, Tokyo, 158-0082, Japan; [2] SOITEC Asia, 3-3-1 Marunouchi, Chiyoda-ku, Tokyo, 100-0005, Japan; [3] Musashi Institute of Technology, 8-15-1 Todoroki, Setagaya-ku, Tokyo, Japan

3:30: 15B.4 **Interdiffusion in SiGe/Si Epitaxial Heterostructures**, Guangrui Xia[1]; Michael Canonico[2]; Judy L Hoyt[1]; [1] Microsystems Technology Laboratories, Massachusetts Institute of Technology, 60 Vassar Street, Rm. 39-661, Cambridge, MA, 02139, USA; [2] Physical Analysis Laboratory Arizona (PALAZ), Freescale Semiconductor, Inc., Tempe, AZ, 85284, USA